40Gb/s QSFP+ Passive Copper Cable

APCP04QQCXXX-XX

■ Product Features

✓ Available in lengths of 1 to 5m

✓ 4 independent full-duplex channels up

   To 11.3Gbps data rate per wavelength

✓ Hot-pluggable QSFP +footprint

✓ RoHS compliant and Lead Free

✓ Power dissipation <0.1W (0~70℃)

✓ Commercial operating temperature optional

✓ Compliant with IEEE802.3ba, SFF-8436

■ Applications

✓ 40G Ethernet

✓ Infiniband 4X SDR DDR QDR

✓ 40G Telecom connections

■ Product Selection

Part Number	Lengths	Wire Size
APCP04-QQC010-30	1m	AWG30
APCP04-QQC020-30	2m	AWG30
APCP04-QQC030-30	3m	AWG30
APCP04-QQC050-26	5m	AWG26

*For availability of additional cable lengths, please contact ATOP.

■ **Regulatory Compliance**

● ESD to the Electrical PINs: compatible with MIL-STD-883 Method 3015

● Immunity compatible with IEC 61000-4-3

● EMI compatible with FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B

● RoHS compliant with RoHS 2 (2011/65/EU)

■ **Pin Descriptions**

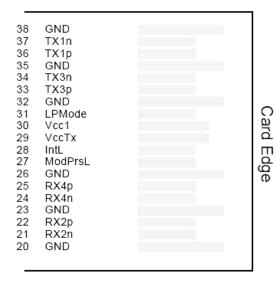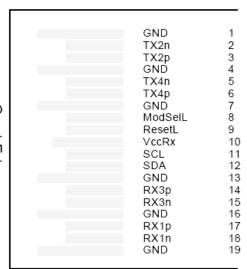| Pin	Symbol	Name/Description	Ref.
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input, CML-I	
3	Tx2p	Transmitter Non-Inverted Data output, CML-I	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input, CML-I	
6	Tx4p	Transmitter Non-Inverted Data output, CML-I	
7	GND	GND	
8	ModSelL	The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the "High" state in the module	
9	ResetL	The ResetL pin must be pulled to Vcc in the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released.	
10	VccRx	+ 3.3V Power Supply Receiver	
11	SCL	2-Wire Serial Interface Clock	
12	SDA	2-Wire Serial Interface Data	
13	GND	GND	
14	Rx3p	Receiver Non-Inverted Data Output, CML-O	
15	Rx3n	Receiver Inverted Data Output, CML-O	

16	GND	GND	
17	Rx1p	Receiver Non-Inverted Data Output, CML-O	
18	Rx1n	Receiver Inverted Data Output, CML-O	
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output, CML-O	
22	Rx2p	Receiver Non-Inverted Data Output, CML-O	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output, CML-O	
25	Rx4p	Receiver Non-Inverted Data Output, CML-O	
26	GND	Ground	
27	ModPrsL	Module Present, connect to GND	
28	IntL	The IntL pin is an open collector output and must be pulled to host supply voltage on the host board. The INTL pin is de-asserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read.	
29	VccTx	+3.3 V Power Supply transmitter	
30	Vcc1	+3.3 V Power Supply	
31	LPMode	The LPMode pin shall be pulled up to Vcc in the QSFP+ module. This function is affected by the LPMode pin and the combination of the Power_over-ride and Power_set software control bits (Address A0h, byte 93 bits 0,1).	
32	GND	Ground	
33	Tx3p	Transmitter Non-Inverted Data Input, CML-I	
34	Tx3n	Transmitter Inverted Data Output, CML-I	
35	GND	Ground	
36	Tx1p	Transmitter Non-Inverted Data Input, CML-I	
37	Tx1n	Transmitter Inverted Data Output, CML-I	
38	GND	Ground	

Top Side Viewed from Top

38	GND
37	TX1n
36	TX1p
35	GND
34	TX3n
33	TX3p
32	GND
31	LPMode
30	Vcc1
29	VccTx
28	IntL
27	ModPrsL
26	GND
25	RX4p
24	RX4n
23	GND
22	RX2p
21	RX2n
20	GND

Card Edge

Bottom Side Viewed from Bottom

GND	1
TX2n	2
TX2p	3
GND	4
TX4n	5
TX4p	6
GND	7
ModSelL	8
ResetL	9
VccRx	10
SCL	11
SDA	12
GND	13
RX3p	14
RX3n	15
GND	16
RX1p	17
RX1n	18
GND	19

Pin-out of Connector Block on Host Board

■ Recommend Circuit Schematic

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		+4.0	V	
Storage Temperature	TS	-40		+85	°C	
Operating Humidity	RH	0		85	%	

■ Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Power Supply Voltage	Vcc	3.13	3.30	3.47	V	
Power Supply Current	Icc	-	-	0.03	A	Commercial
Case Operating Temperature	Tc	0	-	+70	°C	Commercial
Bit Rate Each Lane	Br	1	-	11.3	Gbps	

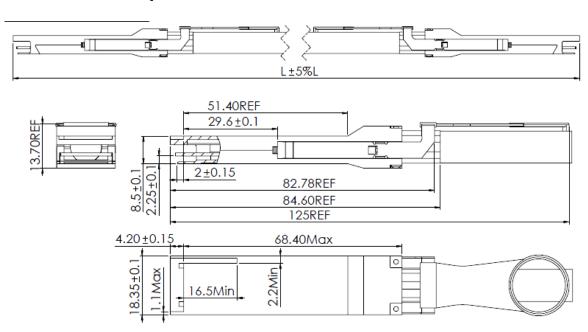## ■ Electrical Characteristics (TOP=25°C, Vcc=3.3Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Input differential impedance	Rin	80	100	120	Ω	
Receiver						
Output differential impedance	Rout	80	100	120	Ω	
S Parameters (10GSFP+Cu Cable Assembly Specifications at B' and C')						
Differential Output/Input Reflection Coefficient	SDDxx			$-12 + 2 \times SQRT(f)$	dB	1
				$-6.3 + 13 \times log10(f/5.5)$	dB	2
Common Mode Output/Input Reflection Coefficient	SCCxx			$-7 + 1.6 \times f$	dB	3
				-3	dB	4

Note:

1: 0.01-4.1 GHz, reference differential impedance is 100 Ω. The dB value listed here are the same as dBe.

2: 4.1-11.1 GHz, reference differential impedance is 100 Ω. The dB value listed here are the same as dBe.

3: 0.01-2.5 GHz, reference differential impedance is 25 Ω. The dB value listed here are the same as dBe.

3: 2.5-11.1 GHz, reference differential impedance is 25 Ω. The dB value listed here are the same as dBe.
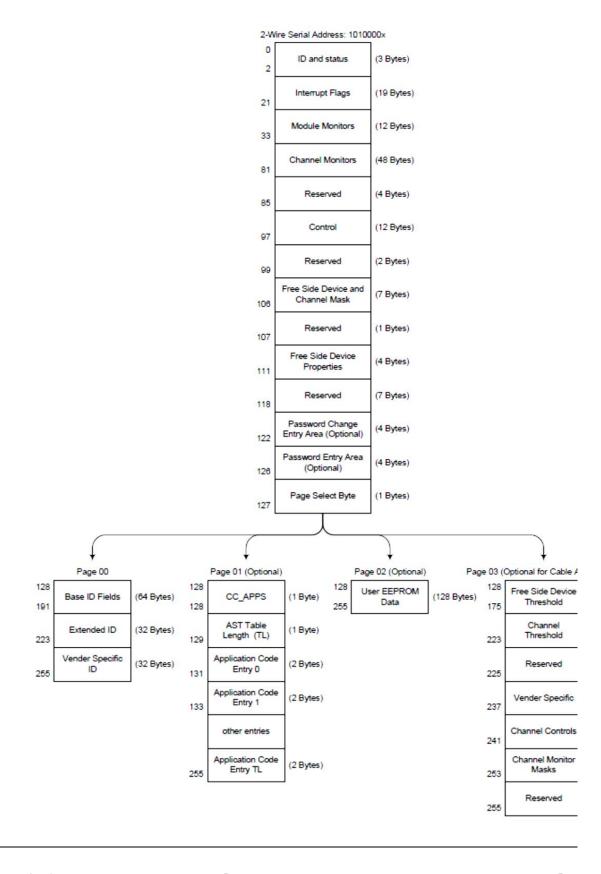
■ Mechanical Specifications

APCP04-QQCXXX-XX

Parameter	Symbol	Min	Typ	Max	Unit
Durability		100			cycle
Transceiver Insert Force		40			N
Transceiver Extraction Force		11.5			N
Transceiver Retention Force		90		170	N

■ **EEPROM Information**

EEPROM memory map specific data field description is as below:

2-Wire Serial Address: 1010000x

Offset	Field	Size
0 – 2	ID and status	(3 Bytes)
2 – 21	Interrupt Flags	(19 Bytes)
21 – 33	Module Monitors	(12 Bytes)
33 – 81	Channel Monitors	(48 Bytes)
81 – 85	Reserved	(4 Bytes)
85 – 97	Control	(12 Bytes)
97 – 99	Reserved	(2 Bytes)
99 – 106	Free Side Device and Channel Mask	(7 Bytes)
106 – 107	Reserved	(1 Bytes)
107 – 111	Free Side Device Properties	(4 Bytes)
111 – 118	Reserved	(7 Bytes)
118 – 122	Password Change Entry Area (Optional)	(4 Bytes)
122 – 126	Password Entry Area (Optional)	(4 Bytes)
126 – 127	Page Select Byte	(1 Bytes)

Page 00

Offset	Field	Size
128 – 191	Base ID Fields	(64 Bytes)
191 – 223	Extended ID	(32 Bytes)
223 – 255	Vender Specific ID	(32 Bytes)

Page 01 (Optional)

Offset	Field	Size
128 – 128	CC_APPS	(1 Byte)
128 – 129	AST Table Length (TL)	(1 Byte)
129 – 131	Application Code Entry 0	(2 Bytes)
131 – 133	Application Code Entry 1	(2 Bytes)
133 –	other entries	
– 255	Application Code Entry TL	(2 Bytes)

Page 02 (Optional)

Offset	Field	Size
128 – 255	User EEPROM Data	(128 Bytes)

Page 03 (Optional for Cable A

Offset	Field
128 – 175	Free Side Device Threshold
175 – 223	Channel Threshold
223 – 225	Reserved
225 – 237	Vender Specific
237 – 241	Channel Controls
241 – 253	Channel Monitor Masks
253 – 255	Reserved

■ Digital Diagnostic Monitoring Interface

None.

■ Revision History

Revision	Initiated	Reviewed	Approved	DCN	Release Date
V1.0	Cade.chen	Tang zhigiang	Ding zheng	New Released.	Mar 28, 2016

■ For More Information

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